ISL75052SEH High Performance 3A LDO Evaluation Board User Guide

Description

The ISL75052SEH is a high-performance, adjustable, low-voltage, high-current, low-dropout linear regulator specified at 1.5A rated output current for input voltages from 4.0V to 13.2V. The LDO outputs can be adjusted from 0.6V to 12.7V by means of two preset resistors. Salient features of the part include:

- TID, ELDRS and SEE Rated
- Very Fast Load Transient Response
- ±2.0% Guaranteed V_{OUT} Accuracy over Line, Load and Temperature
- Typical Dropout of 225mV at 1.5A
- EN Feature
- PG Feature
- OCP Feature
- Short-circuit and Over-temperature Protection

The ISL75052SEHEVAL1Z evaluation board provides a simple platform to evaluate performance of the ISL75052SEH. The device output voltage is adjustable, and jumpers are provided to easily set popular output voltages.

What's Inside

The evaluation kit contains the following:

- ISL75052SEHEVAL1Z evaluation board
- ISL75052SEH datasheet
- AN1850 application note

Test Steps

1. Select the desired output voltage by shorting one of the jumpers from J1 through J5. The option of JP6 provides for continuous adjustment of V_{OUT} using potentiometer R6.
2. Set the OCP limit by using jumpers JP8 and JP9. JP9 = 0.275A min, and JP8 = 2.75A min.
3. Close JP7. Also closing jumper JP11 (2 and 3) selects R16 = 5.49k as pull-up for PGOOD. Close JP12 (1 and 2).
4. Connect the input supply to V_{IN}/GND and the load to V_{OUT}/GND. Select the V_{IN} to V_{OUT} ratio to keep dissipation within the thermal limits of the device.
5. Use JP10 to enable/disable the IC; Open = Enable, and Close = Disable. (Note: For REVB boards, Close = Enable and Open = Disable.)

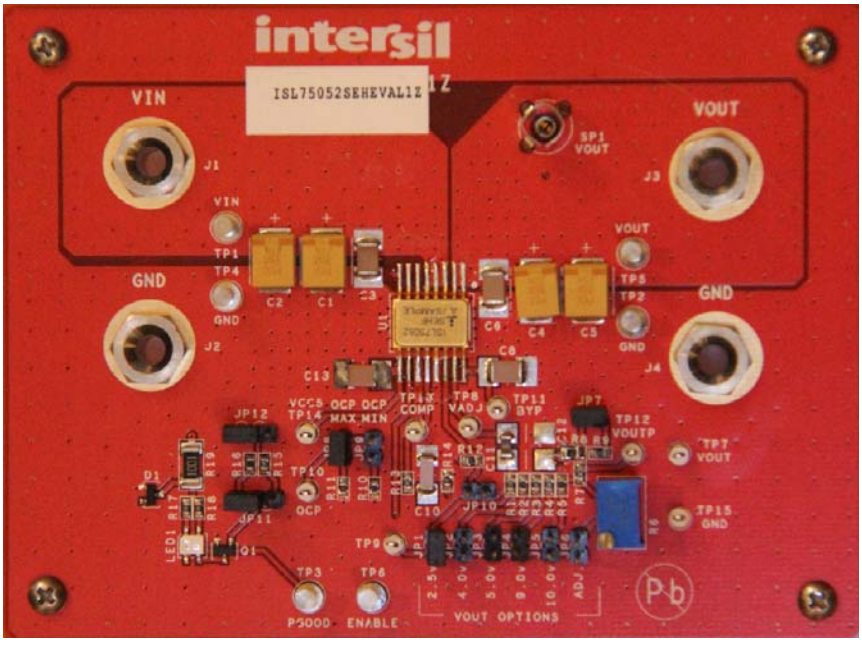


FIGURE 1. ISL75052SEHEVAL1Z EVALUATION BOARD

Optimizing LDO Performance

Performance of the ISL75052SEH can be optimized by following the guidelines provided in this application note.

Input and Output Capacitor Selection

RH operation requires the use of a combination of tantalum and ceramic capacitors to achieve a good volume-to-capacitance ratio. The recommended combination is a 2x100µF, 60mΩ, 25V KEMET T541 series tantalum capacitor in parallel with a 0.1µF MIL-PRF-49470 CDR04 ceramic capacitor. This is to be connected between V_{IN} to GND pins and V_{OUT} to GND pins of the LDO, with PCB traces no longer than 0.5cm. The stability of the device depends on the capacitance and ESR of the output capacitor. The usable ESR range for the device is 6mΩ to 100mΩ. At the lower limit of ESR = 6mΩ, the phase margin is about 51°C. On the high side, an ESR of 100mΩ is found to limit the gain margin at around 10dB. The typical GM/PM seen on the ISL75052SEHEVAL1Z evaluation board for V_{IN} = 3.3V, V_{OUT} = 1.8V, and I_{OUT} = 3A, with a 220µF, 10V, 25mΩ capacitor, is GM = 16.3dB and PM = 69.16°C.

Output Voltage Adjustment

The output voltage can be adjusted by means of the resistor divider shown in Figure 2 as R_{TOP} and R_{BOTTOM}.

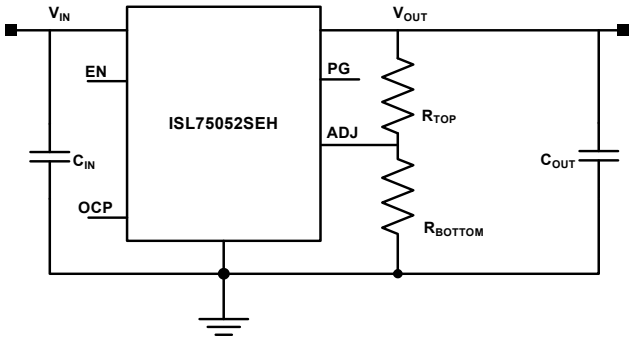


FIGURE 2. ISL75052SEH TYPICAL APPLICATION

The resistor values for typical output voltages are given in Table 1. The values listed provide for an Evaluation board output voltage that is about 50mV higher than the desired set point to allow for the drop on the line connecting the Evaluation board to the desired load.

The resistor divider values can be calculated using the equation:

$V_{OUT} = (0.6X(1+R_{TOP}/R_{BOTTOM})$

Assuming a value R_{TOP} = 15.8k and knowing the required output voltage setting one can calculate the R_{BOTTOM}.

TABLE 1. RECOMMENDED OUTPUT CAPACITOR VALUES

V_{OUT} (V)	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	C_{OUT} (µF)
10.0	15.8	1.0	200
9.0	15.8	1.13	200
5.0	15.8	2.15	200
4.0	15.8	2.74	200
2.5 (Note 1)	15.8	4.87	47
2.5	15.8	4.87	200

NOTE:

1. Either option could be used depending on cost/performance requirements.

Layout Guidelines

Good PCB layout is important to achieving expected performance. When placing components and routing traces, minimize ground impedance and keep parasitic inductance low. Give the input and output capacitors a good ground connection, and place them as close to the IC as possible. Route the traces connecting the ADJ pin away from noisy planes and traces, and keep the board capacitance of the ADJ net to GND as low as possible.

Thermal Guidelines

If the die temperature exceeds +175°C typical, then the LDO output shuts down to zero until the die temperature cools to +155°C typical. The level of power combined with the thermal impedance of the package (θ_{JC} of 4°C/W for the 18 Ld CDFP package) determines whether the junction temperature exceeds the thermal shutdown temperature specified in the “Electrical Specifications” table of the ISL75052SEH datasheet. Mount the device on a high effective thermal conductivity PCB with thermal vias, per JESD51-7 and JESD51-5. Place a silpad between package base and PCB copper plane. Select the V_{IN} and V_{OUT} ratios to ensure that dissipation for the selected V_{IN} range keeps T_J within the recommended operating level of 150°C for normal operation.

Typical Performance Curves

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 2.5V$, $C_{IN} = C_{OUT} = 200\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$.

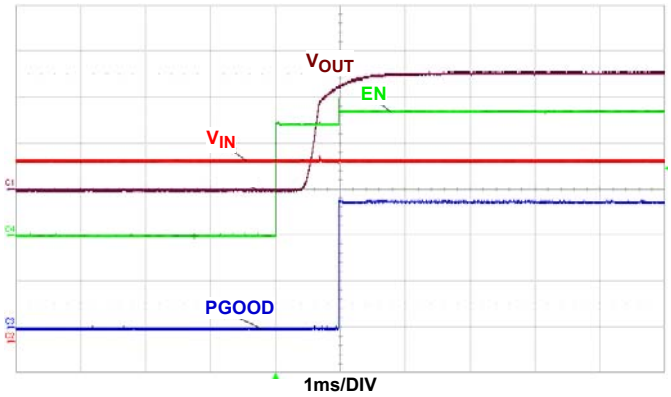


FIGURE 3. START-UP WAVEFORMS: $V_{IN} = 4.0V$, $V_{OUT} = 2.5V$, $I_{OUT} = 0.1A$, EN LOW TO HIGH

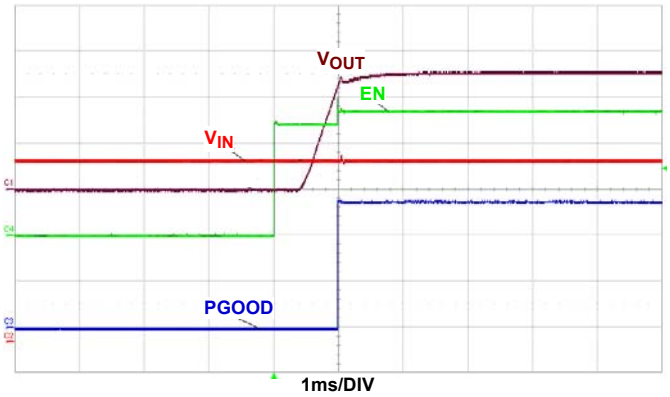


FIGURE 4. START-UP WAVEFORMS: $V_{IN} = 4.0V$, $V_{OUT} = 2.5V$, $I_{OUT} = 1.5A$, EN LOW TO HIGH

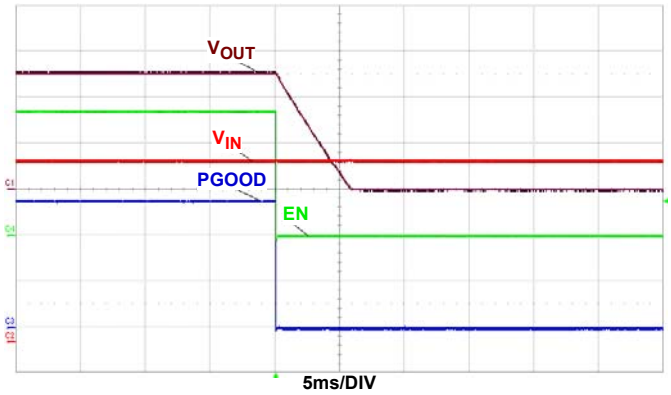


FIGURE 5. SHUTDOWN WAVEFORM: $V_{IN} = 4.0V$, $V_{OUT} = 2.5V$, $I_{OUT} = 0.1A$ EN HIGH TO LOW

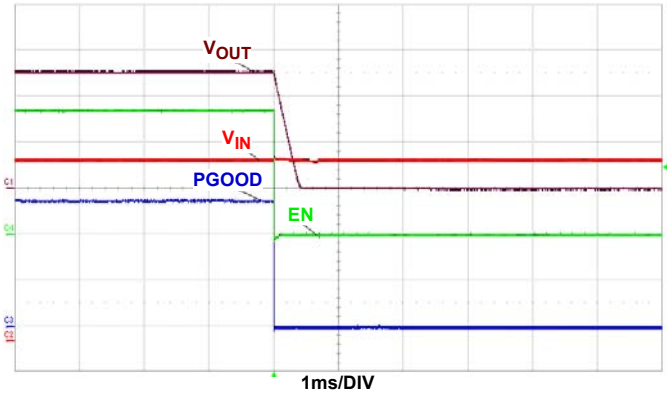


FIGURE 6. SHUTDOWN WAVEFORM: $V_{IN} = 4.0V$, $V_{OUT} = 2.5V$, $I_{OUT} = 1.5A$, EN HIGH TO LOW

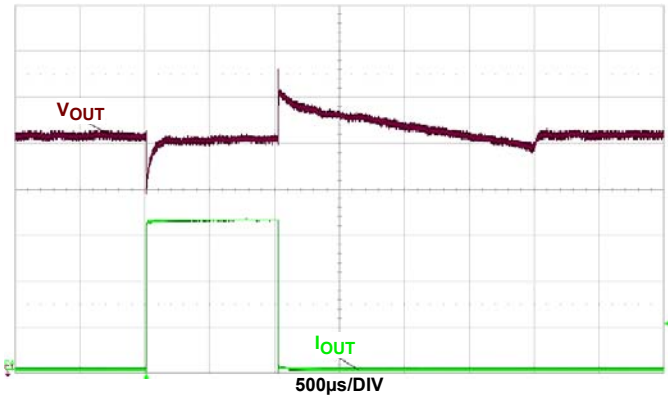


FIGURE 7. LOAD TRANSIENT, $V_{IN} = 13.2.0V$, $V_{OUT} = 10.0V$, $I_{OUT} = 0A$ TO $1.6A$, $C_{OUT} = 200\mu F$ $30m\Omega$

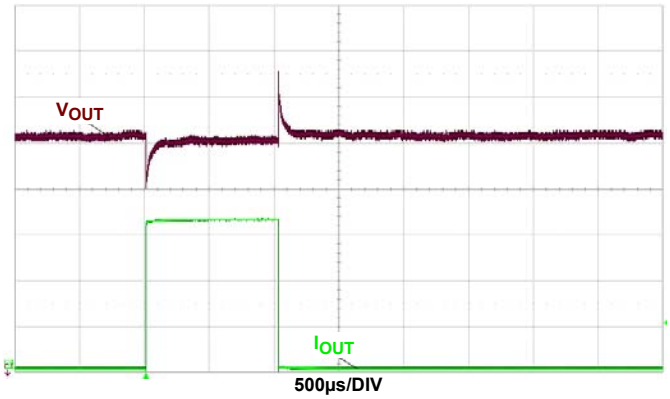


FIGURE 8. LOAD TRANSIENT, $V_{IN} = 13.2V$, $V_{OUT} = 4.0V$, $I_{OUT} = 0.15A$ TO $1.6A$, $C_{OUT} = 200\mu F$ $30m\Omega$

Typical Performance Curves

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 2.5V$, $C_{IN} = C_{OUT} = 200\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$. **(Continued)**

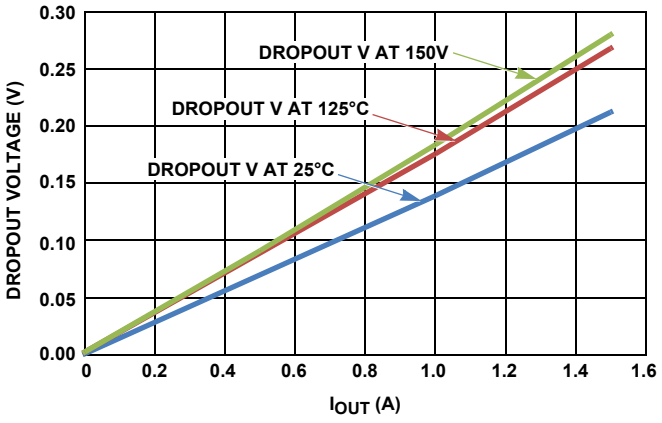


FIGURE 9. DROPOUT vs I_{OUT} AT $V_{OUT} = 3.6V$

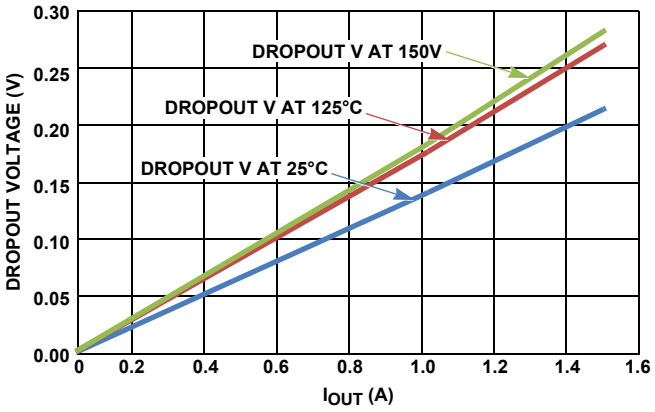


FIGURE 10. DROPOUT vs I_{OUT} AT $V_{OUT} = 12.7V$

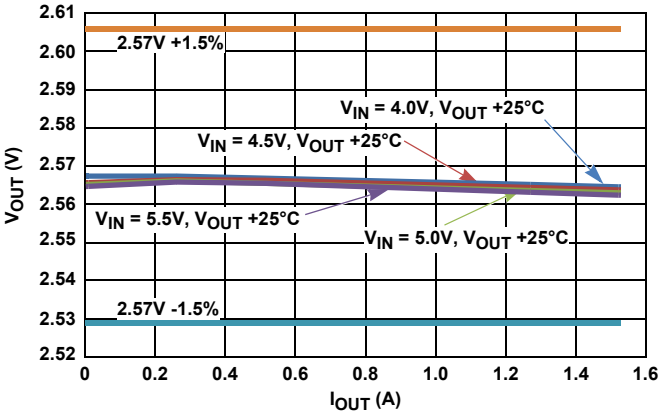


FIGURE 11. LOAD REGULATION V_{OUT} vs I_{OUT}

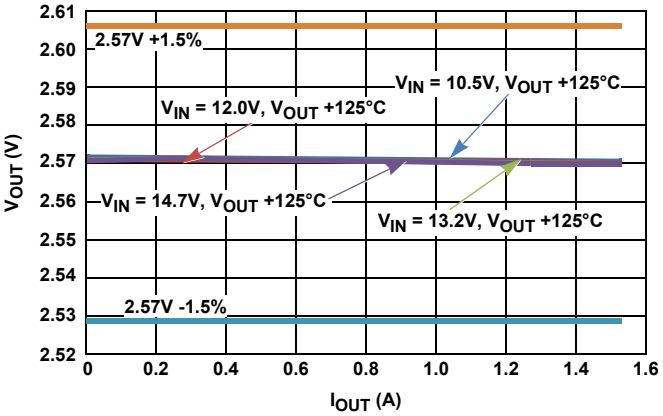


FIGURE 12. LOAD REGULATION V_{ADJ} vs I_{OUT}

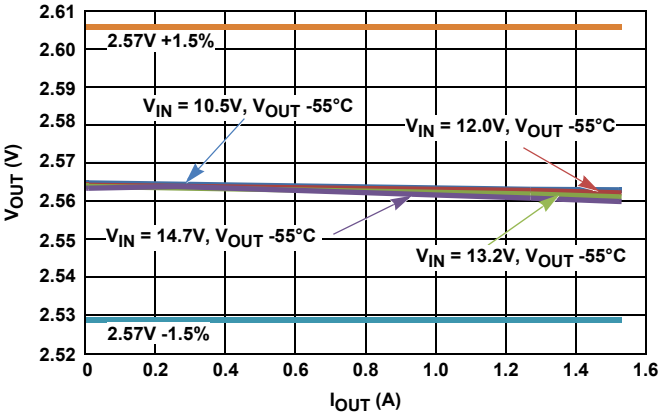


FIGURE 13. LOAD REGULATION V_{OUT} vs I_{OUT}

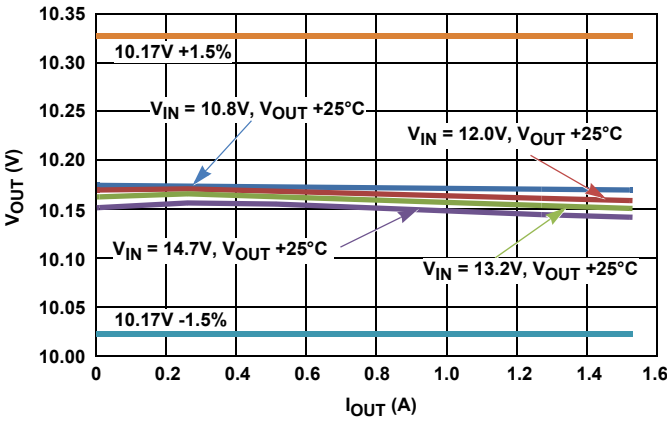


FIGURE 14. LOAD REGULATION V_{ADJ} vs I_{OUT}

Typical Performance Curves

Unless otherwise specified, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 2.5V$, $C_{IN} = C_{OUT} = 200\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$. **(Continued)**

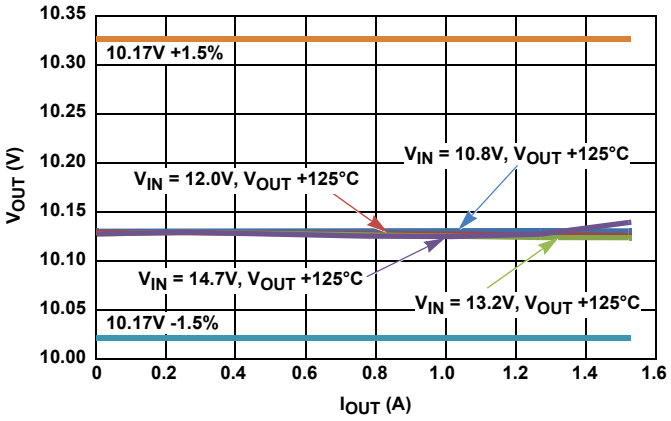


FIGURE 15. LOAD REGULATION V_{OUT} vs I_{OUT}

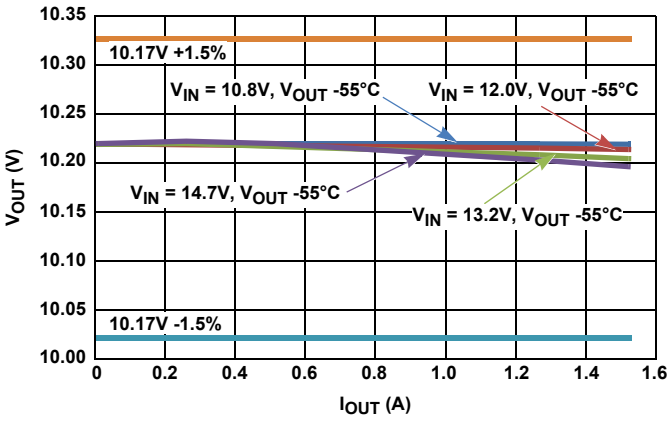


FIGURE 16. LOAD REGULATION V_{ADJ} vs I_{OUT}

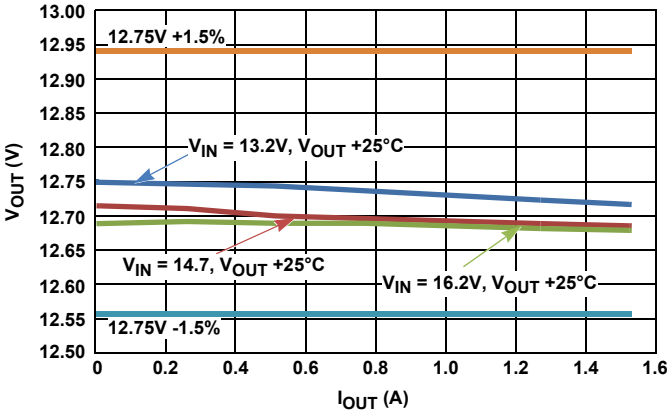


FIGURE 17. LOAD REGULATION V_{OUT} vs I_{OUT}

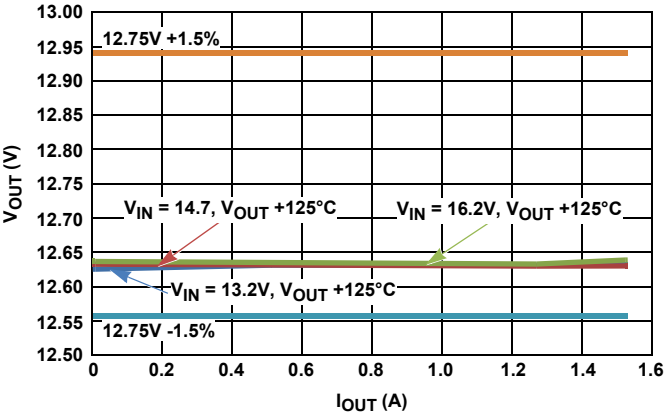


FIGURE 18. LOAD REGULATION V_{OUT} vs I_{OUT}

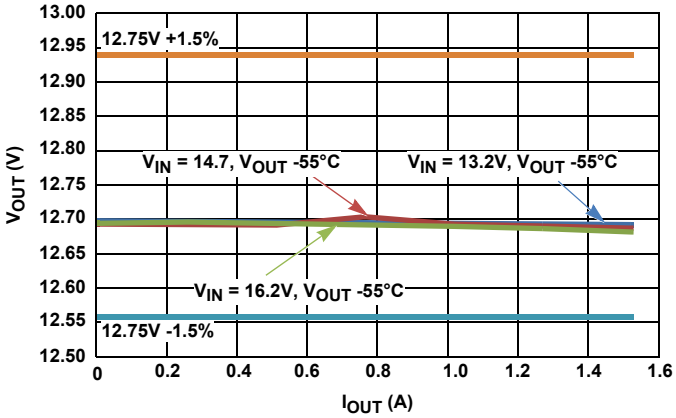
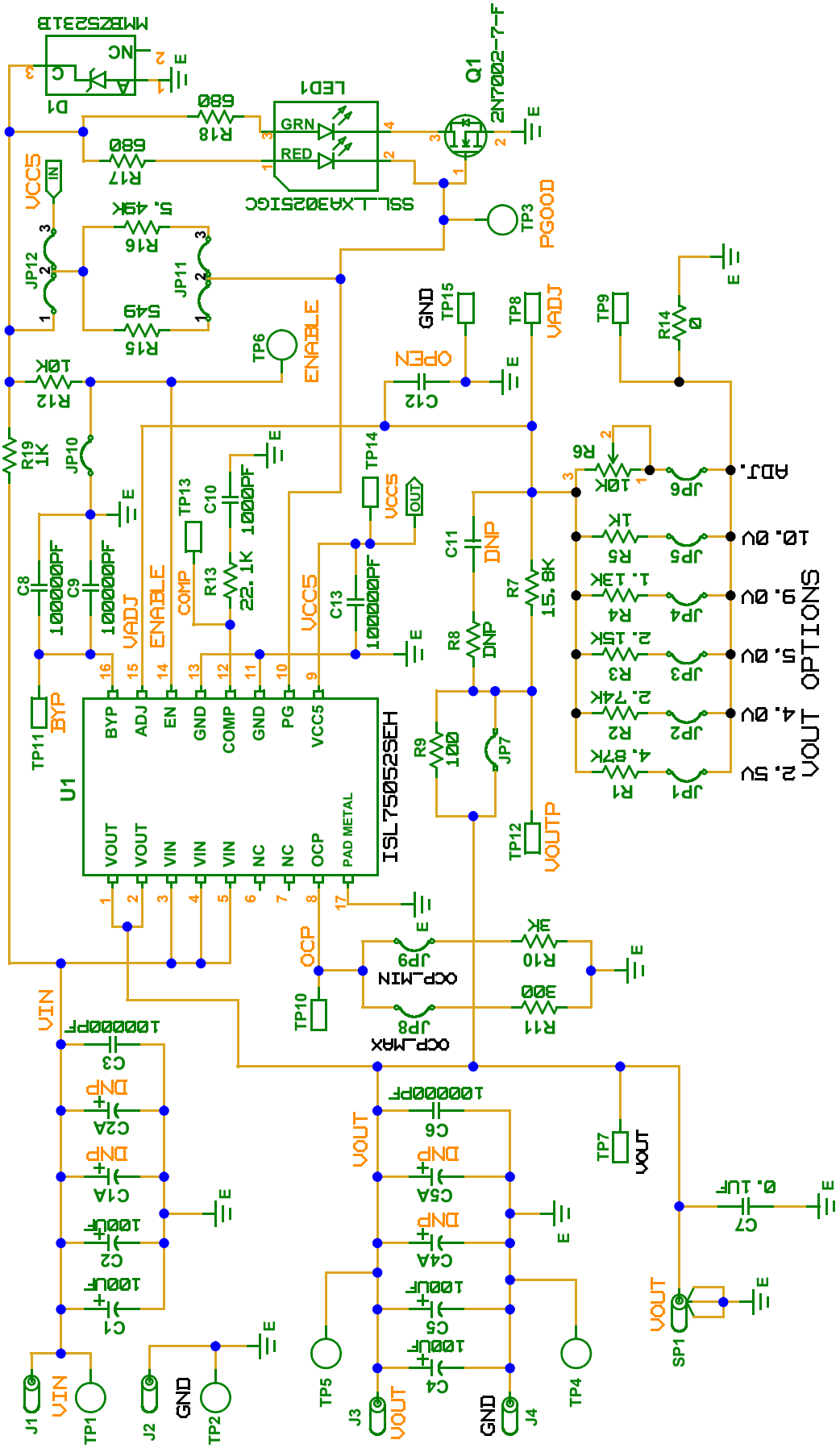


FIGURE 19. LOAD REGULATION V_{OUT} vs I_{OUT}

Schematic


ISL75052SEH
U1
VOUT OPTIONS
2.5V
4.0V
5.0V
9.0V
10.0V
ADJ.
VIN
VOUT
GND
ENABLE
PGOOD
VADJ
VCC5
OCP
OCP_MIN
OCP_MAX
COMP
BYP
LED1
Q1
2N7002-7-F
SSL_LXA3025IGC
MMBZ5231B
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
J1
J2
J3
J4
SP1

Bill of Materials

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MFR	MANUFACTURER PART	MFR
ISL75052SEHEV1ZREVBPCB	1	ea	SEE LABEL-RENAME BOARD	PWB-PCB, ISL75052SEHEV1Z, REVB, ROHS	TBD	ISL75052SEHEV1ZREVBPCB	
CDR03BP102BKMR	1	ea	C10	CAP-MILPRF-55681, SMD, 1808, 0.001µF, 100V, 10%, ROHS	AVX	CDR03BP102BKMR	
CDR04BX104AKMR-T	5	ea	C3, C6, C8, C9, C13	CAP-MILQUAL, SMD, 1812, 0.1µF, 50V, 10%, BX, ROHS	AVX	CDR04BX104AKMR	
H1045-00104-16V10-T	1	ea	C7	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	MURATA	GRM39X7R104K016AD	PANASONIC
T495E107K025ATE100-T	4	ea	C1, C2, C4, C5	CAP-TANT, LOW ESR, SMD, E, 100µF, 25V, 10%, 100mΩ, ROHS	KEMET	T495E107K025ATE100	
108-0740-001	4	ea	J1-J4	CONN-JACK, BANANA-SS-SDRLESS, VERTICAL, ROHS	JOHNSON COMPONENTS	108-0740-001	
131-4353-00	1	ea	SP1	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	TEKTRONIX	131-4353-00	
1514-2	6	ea	TP1-TP6	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2	
5002	9	ea	TP7-TP15	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002	
68000-236HLF-1X3	2	ea	JP11, JP12	CONN-HEADER, 1x3, BREAKAWY 1X36, 2.54mm, ROHS	BERG/FCI	68000-236HLF	
69190-202HLF	10	ea	JP1-JP10	CONN-HEADER, 1X2, RETENTIVE, 2.54mm, 0.230X 0.120, ROHS	BERG/FCI	69190-202HLF	
MMBZ5231B-7-F-T	1	ea	D1	DIODE-ZENER, SMD, SOT-23, 3P, 5.1V, 350mW, ROHS	DIODES INC.	MMBZ5231B-7-F	
SSL-LXA3025IGC-TR	1	ea	LED1	LED, SMD, 3x2.5mm, 4P, RED/GREEN, 12/20MCD, 2V	LUMEX	SSL-LXA3025IGC-TR	
2N7002-7-F-T	1	ea	Q1	TRANSISTOR, N-CHANNEL, 3LD, SOT-23, 60V, 115mA, ROHS	DIODES, INC.	2N7002-7-F	ON SEMICONDUCTOR
3299W-1-103LF	1	ea	R6	POT-TRIM, TH, 3P, 10k, 1/2W, 10%, 3/8SQ, 25TURN, TOPADJ, ROHS	BOURNS	3299W-1-103LF	
H2506-DNP	0	ea	R8	RESISTOR, SMD, 0805, DNP, DNP, DNP, TF			
H2511-00R00-1/10W-T	1	ea	R14	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T	ROHM
H2511-01000-1/10W1-T	1	ea	R9	RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1000FT	ROHM

Bill of Materials (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MFR	MANUFACTURER PART	MFR
H2511-01001-1/10W1-T	1	ea	R5	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1001V	VENKEL
H2511-01002-1/10W1-T	1	ea	R12	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	KOA	RK73H1JT1002F	VENKEL
H2511-01131-1/10W1-T	1	ea	R4	RES, SMD, 0603, 1.13k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-071K13L	ROHM
H2511-01582-1/10W1-T	1	ea	R7	RES, SMD, 0603, 15.8k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1582FT	PANASONIC
H2511-02151-1/10W1-T	1	ea	R3	RES, SMD, 0603, 2.15k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-072K15L	VENKEL
H2511-02212-1/10W1-T	1	ea	R13	RES, SMD, 0603, 22.1k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF2212V	VENKEL
H2511-02741-1/10W1-T	1	ea	R2	RES, SMD, 0603, 2.74k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-2741FT	YAGEO
H2511-03000-1/10W1-T	1	ea	R11	RES, SMD, 0603, 300Ω, 1/10W, 1%, TF, ROHS	ROHM	MCR03EZPFX3000	VISHAY/DALE
H2511-03001-1/10W1-T	1	ea	R10	RES, SMD, 0603, 3k, 1/10W, 1%, TF, ROHS	YAGEO	RC0603FR-073KL	VENKEL
H2511-04871-1/10W1-T	1	ea	R1	RES, SMD, 0603, 4.87k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF4871V	VISHAY/DALE
H2511-05490-1/10W1-T	1	ea	R15	RES, SMD, 0603, 549Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5490FT	PANASONIC
H2511-05491-1/10W1-T	1	ea	R16	RES, SMD, 0603, 5.49k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5491FT	YAGEO
H2511-06800-1/10W1-T	2	ea	R17, R18	RES, SMD, 0603, 680Ω, 1/10W, 1%, TF, ROHS	ROHM	MCR03EZPFX6800	VENKEL
H2520-01001-1/2W1-T	1	ea	R19	RES, SMD, 2010, 1k, 1/2W, 1%, TF, ROHS	PANASONIC	ERJ-12SF1001U	VISHAY/DALE
4-40X1/4-SCREW-SS	4	ea	Four corners	SCREW, 4-40X1/4in, PAN, SS, PHILLIPS			
4-40X3/4-STANDOFF-METAL	4	ea	Four corners	STANDOFF, 4-40X3/4in, F/F, HEX, ALUMINUM, ROHS	KEYSTONE	2204 (.250 OD)	
8X8-STATIC-BAG	1	ea	Place assy in bag	BAG, STATIC, 8X8, ZIP LOC, ROHS	ULINE	S-5092	
DNP	0	ea	U1 (ISL75052SEHQF)	DO NOT POPULATE OR PURCHASE			
LABEL-DATE CODE	1	ea		LABEL-DATE CODE_BOM REV#_SERIAL# LABEL ON ZIL & QUEL	INTERSIL	LABEL-DATE CODE	
LABEL-RENAME BOARD	1	ea	RENAME PCB TO: ISL75052SEHEVAL1Z	LABEL, TO RENAME BOARD	INTERSIL	LABEL-RENAME BOARD	

Layout

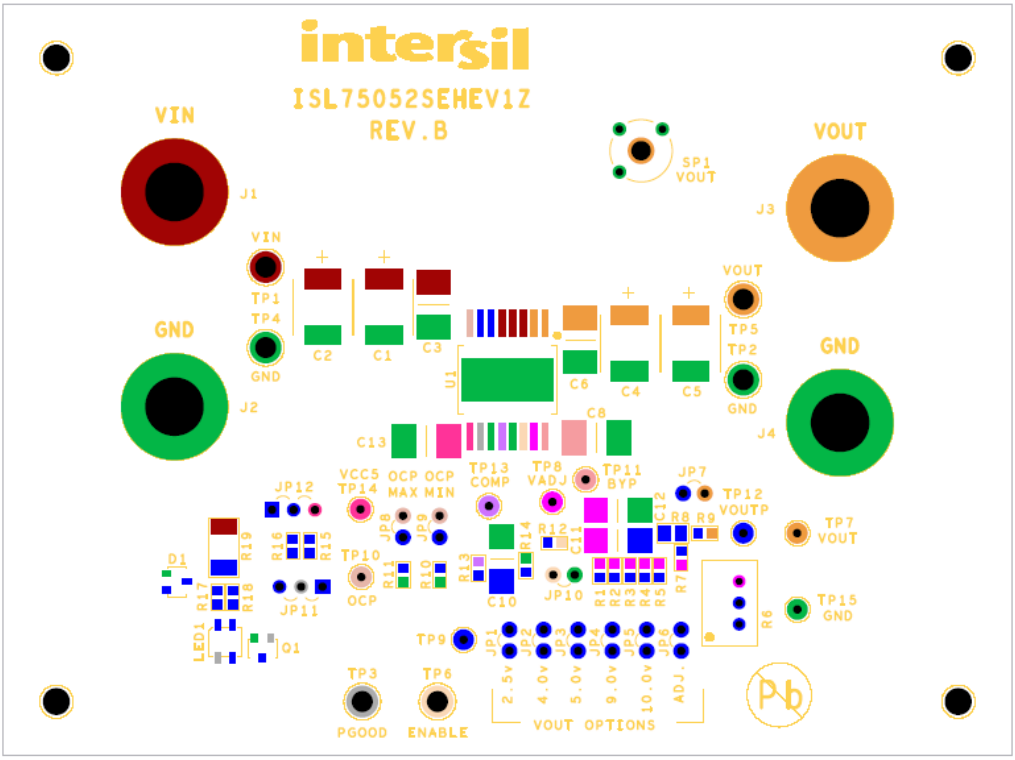


FIGURE 20. SILK SCREEN TOP

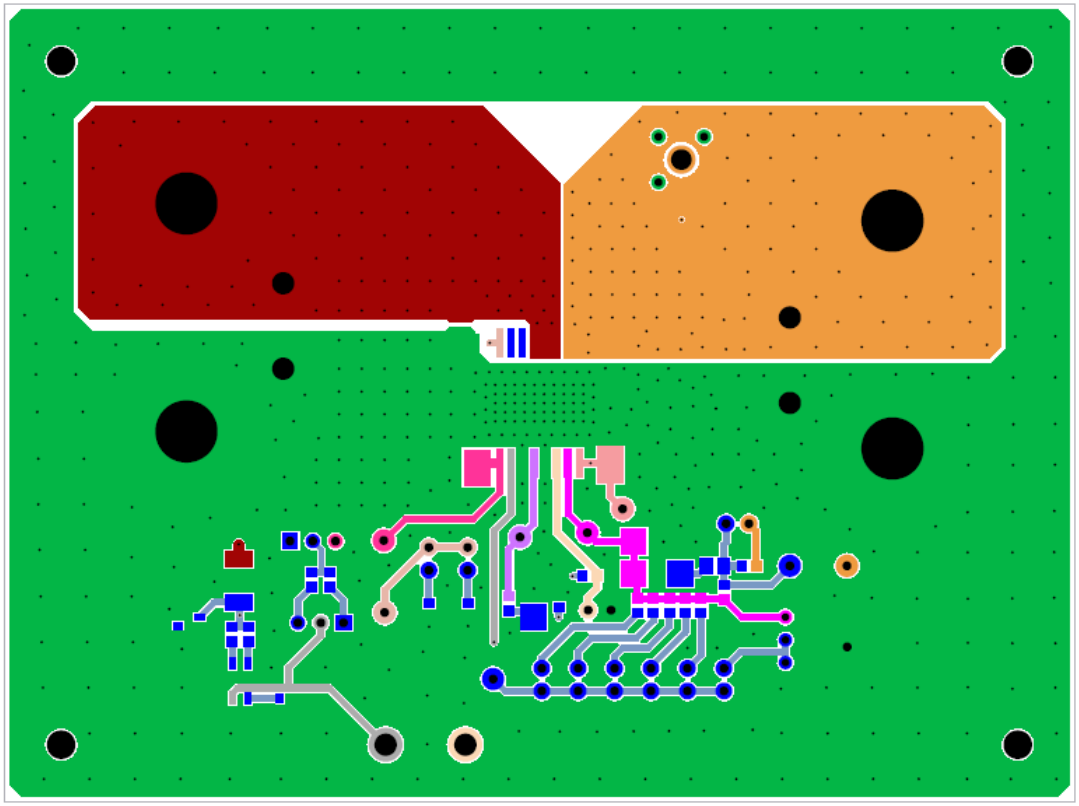


FIGURE 21. TOP LAYER COMPONENT SIDE

Layout (Continued)

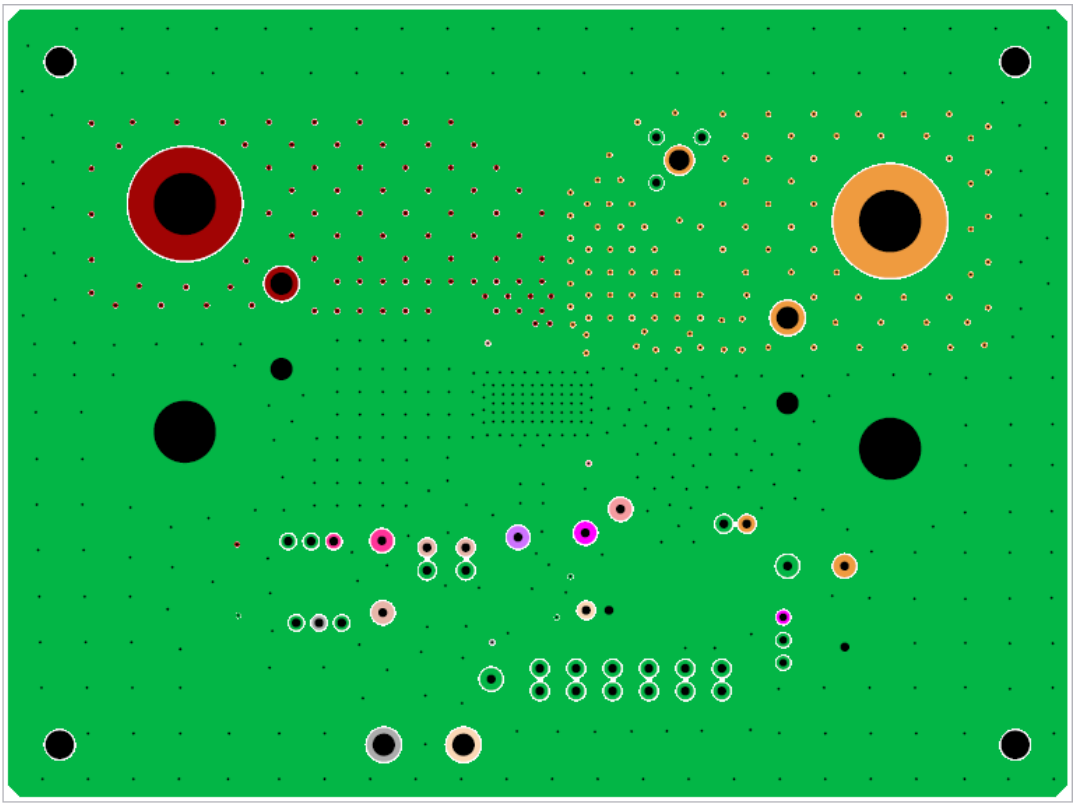


FIGURE 22. LAYER 2

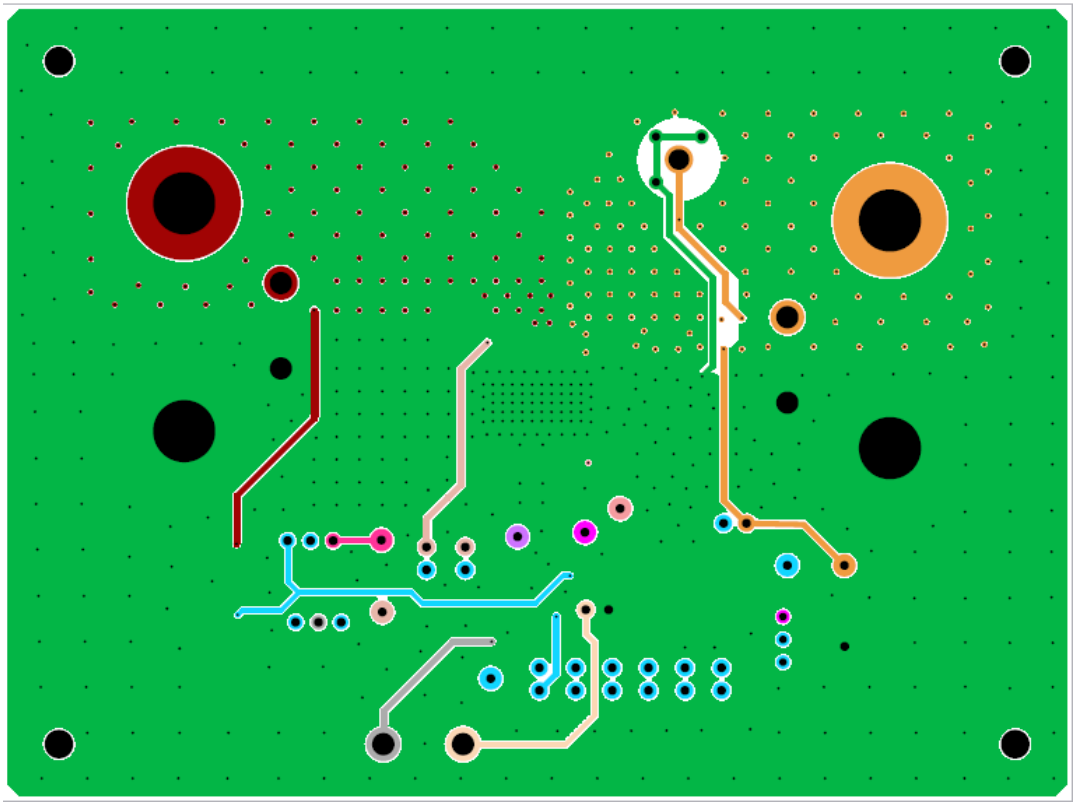


FIGURE 23. LAYER 3

Layout (Continued)

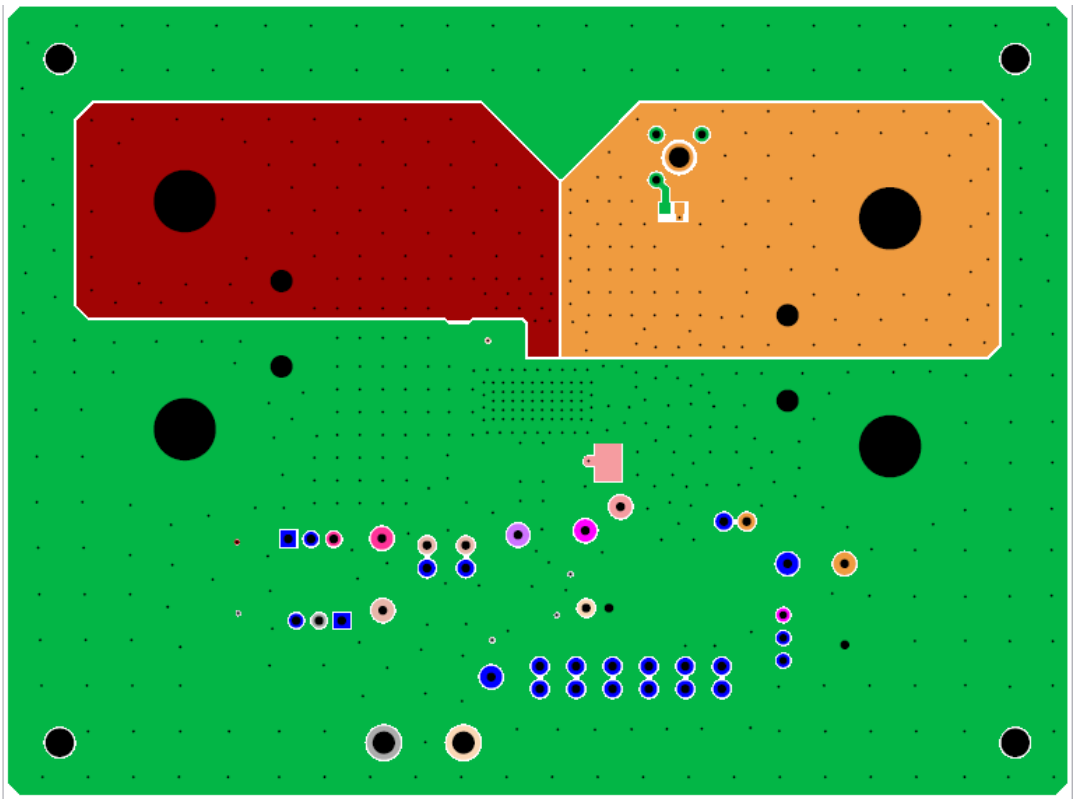


FIGURE 24. BOTTOM LAYER SOLDER SIDE

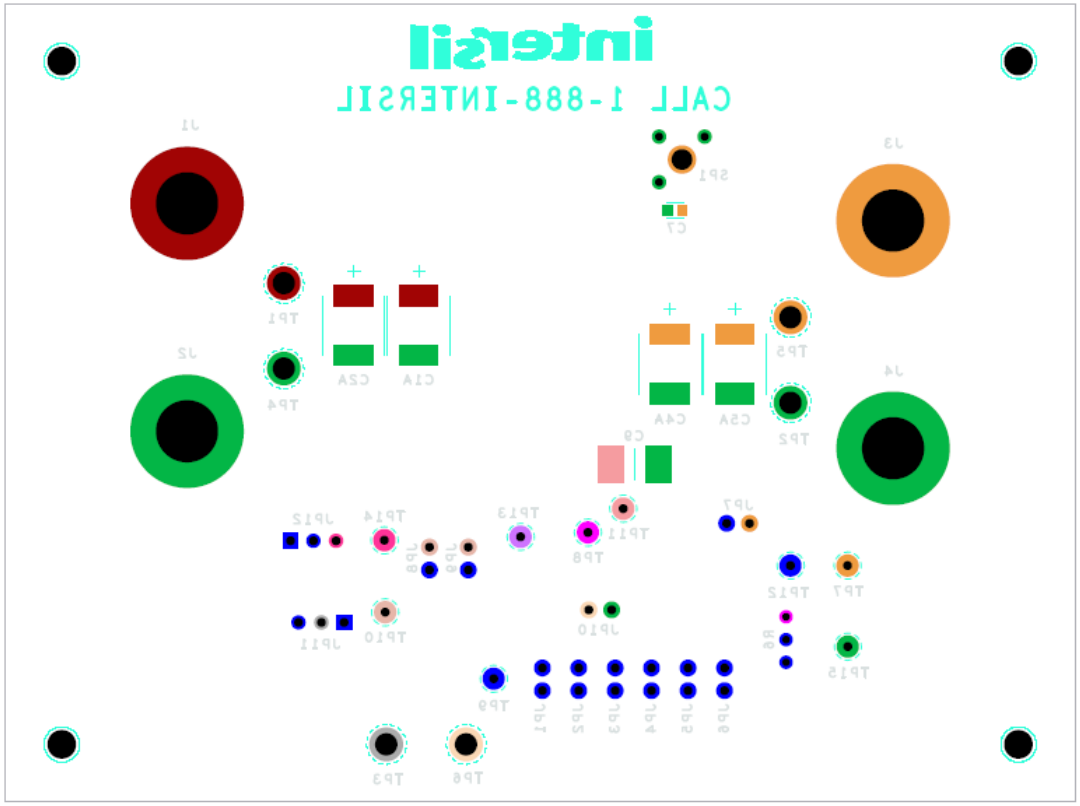


FIGURE 25. SILK SCREEN BOTTOM

Layout (Continued)

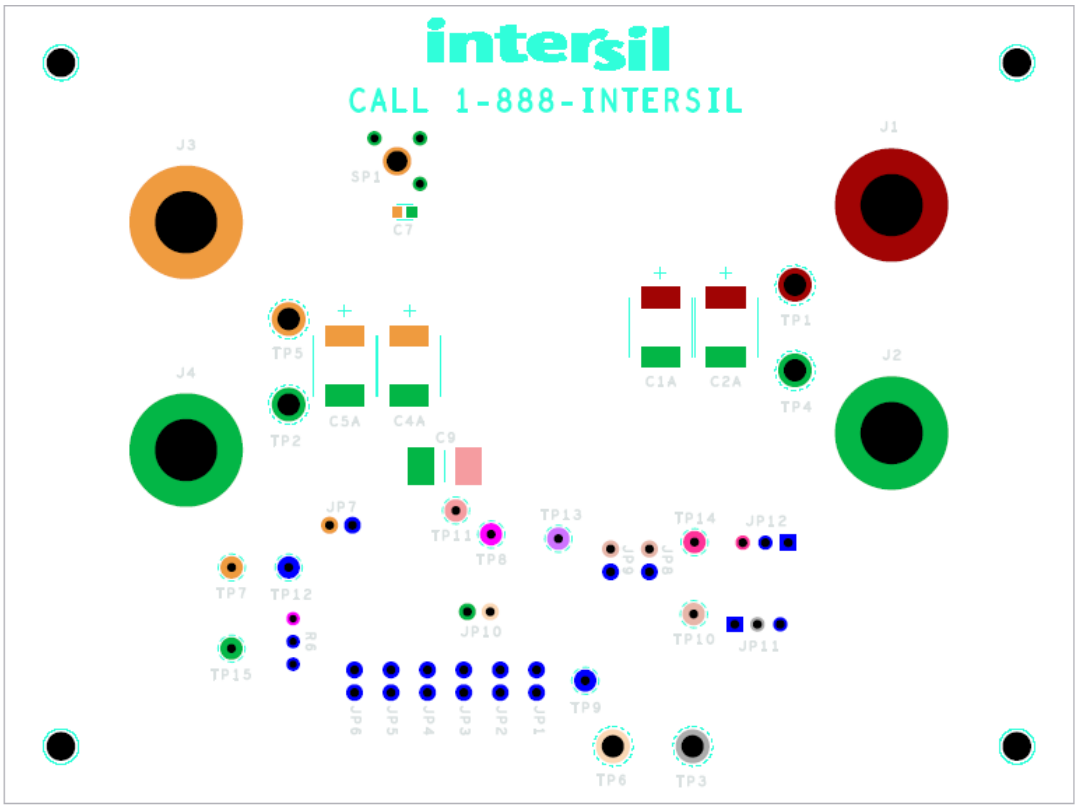
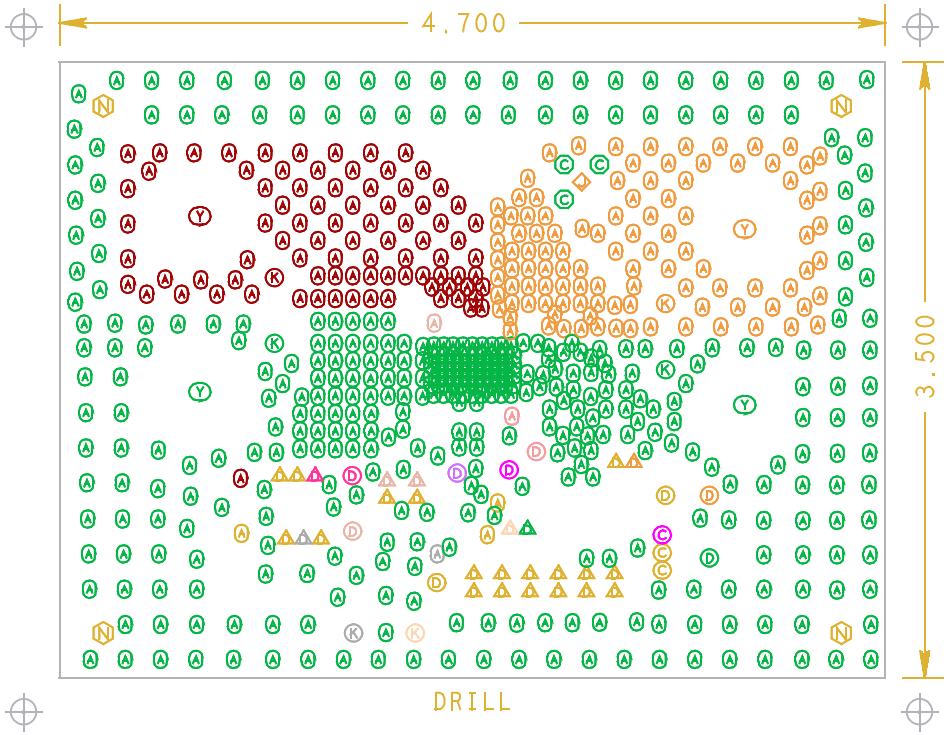


FIGURE 26. SILK SCREEN BOTTOM MIRROR

Drill Drawings



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
Ⓐ	14.0	PLATED	611
Ⓒ	35.0	PLATED	3
Ⓒ	37.0	PLATED	3
Ⓓ	40.0	PLATED	9
Ⓐ	41.0	PLATED	26
◇	93.0	PLATED	1
Ⓚ	100.0	PLATED	6
Ⓨ	275.0	PLATED	4
Ⓝ	128.0	NON-PLATED	4

NOTES:
1. THIS BOARD IS RoHS COMPLIANT.
2. PRINTED WIRING BOARD DESIGN AND ACCEPTANCE CRITERIA SHALL BE IAW WITH THE REQUIREMENTS OF IPC-D-275 AND IPC-A-600.
3. MATERIAL: FR4 (RoHS COMPLIANT), 2 OZ COPPER.
4. APPLY SOLDER MASK, BOTH SIDES OVER BARE COPPER IAW IPC-SM-840. CLASS 2 (LPI) (INTERSIL RED MASK).
5. ALL PATTERNS ARE VIEWED FROM THE PRIMARY SIDE LOOKING THROUGH THE BOARD.
6. UNLESS OTHERWISE SPECIFIED ALL HOLE DIAMETERS ARE AFTER PLATING.
7. APPLY SILKSCREEN USING WHITE NON-CONDUCTIVE EPOXY BASED INK.
8. PWB MUST BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY. USE NETLIST PROVIDED ISL75052SEHEV1ZB_IPC356.IPC IAW IPC-D-356.
9. MARK DATE CODE AND MANUFACTURES IDENIFICATION ON SOLDER SIDE PER IPC-6011 AND IPC-6012.
10 TOLERANCE ON ALL DRILL HOLES SHALL BE IAW IPC-D-2221 & 2222 UNLESS OTHERWISE SPECIFIED.

PHYSICAL BOARD DIMENSIONS
& LAYER STRUCTURE